plurality of said payload data inputs and having a first output and a second output;

a separate exclusive-OR gate having an input coupled to one of said payload data inputs and having an input coupled to said first output of said convolutional encoder and having an output;

a mapper having a plurality of inputs coupled directly to a plurality of said payload data inputs, and having an input coupled to said second output of said convolutional encoder, and having an input coupled to said output of said exclusive-OR gate, and having a plurality of I outputs and a plurality of Q outputs at which signals appear which are constellation points in a quadrature amplitude modulated constellation which are derived from said payload data appearing at said payload data inputs.

2. The apparatus of claim 1 wherein said mapper functions to nonlinearly map the bits input thereto into a constellation point of a 16 QAM constellation.

3. The apparatus of claim 1 wherein three payload bits are received, and wherein said first and second payload bits are applied to said mapper in an unchanged state,, and wherein said convolutional encoder is comprised of a chain of four D type flip flops, the first, second and third of which have their outputs coupled to the input of an exclusive-OR gate which has its output coupled to the input of the next D flip flop in said chain, and the fourth flip-flop having its output coupled to an input of said mapper and to the input of said first flip flop, and wherein the exclusive-OR gate between said first and second flip flops has an input coupled to receive said second payload bit, and wherein said exclusive-OR gate between said second and third flip flops has an input coupled to

receive said first payload bit and an additional input coupled to said output of said separate exclusive-OR gate, and having an additional input coupled to the output of an AND gate which has a first input coupled to the output of said fourth flip flop and a second input coupled to the input of said fourth flip flop, and wherein said third payload bit is modified by said separate exclusive-OR gate by exclusive-OR combination with the output bit from said third flip flop of said convolutional encoder, and wherein said exclusive-OR gate having an input coupled to the output of said third flip flop and an output coupled to the input of said fourth flip flop has an additional input coupled to said output of said separate exclusive-OR gate and an additional input coupled to said output of said fourth flip flop.

4. The apparatus of claim 3 wherein said mapper has at least one control input for receiving control signals which control whether said Trellis encoder operates in a normal mode wherein one redundant bit is added to each three payload bits or a fallback mode wherein the output of said mapper is divided into two symbols and transmitted separately with the two least significant bits (y0, y1) being transmitted as first symbol or constellation point in a QPSK 4-point constellation and the two most significant bits (y3,y2) being transmitted as a second symbol or constellation in a DQPSK constellation.

5. The apparatus of claim 1 wherein said convolutional encoder and separate exclusive-OR gate are structured and coupled together to implement a 16-state convolutional encoding process which only allows certain predetermined patterns in the constellation points that are generated from said payload data bits.

6. The apparatus of claim 1 wherein said convolutional encoder and separate exclusive-OR gate are structured and coupled together so as to be characterized by parity check polynomials given in octal form as follows: h3=04, h2=10, h1=06, h0=23, d^2_free=5.0, Nfree=1.68, and wherein the nonlinear term is given by D^2[y0(S).AND.D^(-1)y0(D)].

7. The apparatus of claim 1 wherein said mapper has multiple modes which add different numbers of redundant bits while always maintaining the code word length at 4 bits including a normal mode where one redundant bit is added per tribit, and a fallback mode which can be used when channel impairments are high wherein fewer payload bits are sent and more redundant bits are sent in each 4 bit code word.

8. An encoder for encoding payload data bits with redundant bits and mapping the resulting bits into a constellation point so as to achieve a coding gain, comprising:

first means for receiving a plurality of payload data bits and convolutionally encoding said payload bits to generate at least one additional bit derived mathematically from a Boolean logic combination of said payload bits, and for outputting at least some of said payload bits unchanged and at least one of said payload bits as modified by a logical operation with a bit output from an intermediate stage of a convolutional encoding process carried out in said first means, and outputting a final bit resulting from said convolutional encoding process; and

second means coupled to receive one or more mode control signals and coupled to receive said final bit from said convolutional encoding process and said

unchanged payload bits and said payload bit after modification by said convolutional encoding process, for mapping said bits into a constellation point of a constellation of possible data points, each point defined by a value on a real axis and a value on an imaginary axis, said mapping having at least a normal mode and a fallback mode .

9. The encoder of claim 8 wherein said first means includes a 16-state convolutional encoder characterized by parity check polynomials given in octal form as follows: h3=04, h2=10, h1=06, h0=23, d^2_free=5.0, Nfree=1.68 and wherein the nonlinear term is given by D^2[y0(S).AND.D^(-1)y0(D)].

10. The encoder of claim 8 wherein said first means and second means implement a forward error correction encoder state machine or lookup table coupled to a state memory which adds at least one extra bit to provide redundancy for error detection and correction and for use by a Viterbi Decoder in a receiver for ascertaining with greater accuracy the data that was actually sent despite the presence of noise, said at least one extra bit providing a constellation that is bigger than the constellation would have without said extra bit(s) thereby enabling more spacing between constellation points thereby enabling better discrimination between points by the receiver and lowering the bit error rate without increasing the bandwidth.

11. A process for Trellis encoding a plurality of payload bits into a constellation point, comprising:

receiving a plurality of payload bits;

convolutionally encoding a combination of said payload bits into one or more additional bits by applying said payload bits to different inputs of a convolutional encoder and also applying a modified bit to an input of said convolutional encoder, said modified bit being generated by exclusive-ORing one of said payload bits with an output bit from an intermediate stage of said convolutional encoder, said convolutional encoding step resulting in output of one or more additional bits; and

mapping the combination of at least some of said payload bits in an unmodified state, said modified bit and said one or more additional bits into a constellation point.

12. The process of claim 11 wherein said process for Trellis encoding is performed upon multiple pluralities of said payload bits successively, and wherein said step of convolutionally encoding comprises introducing a certain dependency between successive constellation points generated from said successive plurality of payload bits such that only certain patterns or permissible sequences of constellation points are permitted, said patterns or permissible sequences capable of being modelled in a receiver's Viterbi decoder as a Trellis code.

13. The process of claim 11 wherein said step of mapping includes the steps of receiving a control signal that indicates whether a normal mode or a fallback mode is to be implemented wherein said normal mode maps said plurality of payload bits, said modified bit and said one or more additional bits into a constellation point in a constellation of points that is larger than a constellation of possible points would be if